REMARKS

Applicants have amended claim 5 to correct a typographic error. The amendment of claim 5 is not made in response to the Examiners rejection of claim 5.

The Examiner rejected claims 1, 8 and 5 under 35 U.S.C. §102(b) as being unpatentable over Morishita et al. (USP 5,757,175).

The Examiner rejected claims 2-4, 13 and 16-17 under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. in view of Mancatis (USP 6,462,527).

The Examiner rejected claims 5, 10, 12 and 18 under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. in view of Mancatis (USP 6,462,527) and Shyr et al. (USP 6,472897).

The Examiner rejected claims 11 and 14 under 35 U.S.C. 103(a) as being unpatentable over Morishita et al.

The Examiner rejected claims 6 and 19 under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. in view of Stubbs et al. (USP 6,597,619).

The Examiner rejected claims 7, 9 and 19 under 35 U.S.C. 103(a) as being unpatentable over Morishita et al. in view of Ngo et al. (USP 5,942,934).

Applicants respectfully traverse the 35 U.S.C. §102(b) and §103(a) rejections with the following arguments.

35 USC § 102

As to claims 1, 8 and 15, the Examiner states that "Morishita et al. discloses in figure 7 a circuit, and a method thereof, comprising, comprising a current mirror (2,NT2) coupled to a tunneling leakage monitor (PT3, PT4 and circuit CVC in figure 6), the tunneling leakage monitor including a tunneling leakage monitoring device (in the CVC), the current mirror adapted to force a tunneling leakage current of the tunneling leakage device to a predetermined current value; and a voltage buffer (CMP and DT in figure 6) coupled to the leakage monitor, the voltage buffer adapted to generate an output voltage (INVCC) based on a voltage level developed across the leakage monitoring device when the tunneling leakage current is at the predetermined current value."

Applicants contend that claim 1, as amended, is not anticipated by Morishita et al. because Morishita et al. does not teach each and every feature of claim 1. As a first example Morishita et al. does not teach "a tunneling leakage monitor." As a second example, Morishita et al. does not teach "said tunneling leakage monitor including a tunneling leakage monitoring device." As a third example, Morishita et al. does not teach "said current comprising only tunneling leakage current." Applicants respectfully point out that the circuit comprising PT3, PT4 and circuit CVC (current to voltage converter) in figure 6 of Morishita et al. cannot function as "a tunneling leakage monitor" 1 nor do the CVCs of Morishita et al. include "a tunneling leakage monitoring device" as the Examiner alleges and Applicants claim 1 requires.

Applicants have found only one example of the CVC circuit in Morishita et al. and that in FIG. 19 and described in col. 4 lines 11-18 of Morishita et al. which states in part "CVC includes p-channel MOS transistors Pra...PRb and PRc connected in series between current output node and the ground node." FIG. 19 of Morishita et al. clearly shows the gates of PFETs

Pra...PRb and PRc coupled to ground. The PFET's Pra...PRb and PRc of Morishita et al. are biased in the linear region of the PFETs and thus act as resistors. The current flow through the CVC from Vref to ground is overwhelmingly a source to drain current over three orders in magnitude greater than any possible leakage current that could flow to ground. Not only is the current through the CVC not "only tunneling leakage current" as Applicants claim 1 requires, but any leakage current through these PFETs would be so small a percentage of total current that the CVC would be insensitive to changes in leakage current and is thus not capable as functioning as "a tunneling current monitor" as Appplicants claim 1 requires.

Applicants contend that claim 8, as amended, is not anticipated by Morishita et al. because Morishita et al. does not teach each and every feature of claim 1. For example Morishita et al. does not teach "forcing a current of known value only through a dielectric layer of a tunneling current leakage monitor device to provide a voltage signal." Applicants believe the arguments provided *supra* with respect to claim 1 are applicable to claim 8. Further, Applicants point out that Morishita et al. does not mention tunneling currents and therefore can not have anticipated a method requiring "forcing a current of known value through a tunneling leakage monitor device" as Applicants claim 8 requires.

Applicants contend that claim 15, as amended, is not anticipated by Morishita et al. because Morishita et al. does not teach each and every feature of claim 15. As a first example Morishita et al. does not teach "a tunneling leakage monitor." As a second example, Morishita et al. does not teach "said tunneling leakage monitor including a tunneling leakage monitoring device." As a third example, Morishita et al. does not teach "said current comprising only tunneling leakage current." Applicants believe the arguments provided *supra* with respect to claims 1 and 8 are applicable to claim 15.

Based on the preceding arguments, Applicants respectfully maintain that claims 1, 8 and 15 are not unpatentable over Morishita et al. and are in condition for allowance. Since claims 2-7 depend from claim 1, claims 9-14 depend from claim 8 and claims 16-20 depend from claim 15, Applicants respectfully maintain that claims 2-7, 9-14 and 16-20 are likewise in condition for allowance.

35 USC § 103 Rejections

As to claims 2, 3, 13 and 16, since claims 2 and 3 depend from claim 1, claim 13 depends from claim 8 and claim 16 depends from claim 15, which Applicants have argued *supra* to not be unpatentable over Morishita et al. under 35 U.S.C. §102(b), Applicants maintain that claims 2, 3, 13 and 16 are likewise not unpatentable over Morishita et al. in view of Mancatis under 35 U.S.C. §103(a).

As to claims 5, 10, 12 and 18, since claim 5 depends from claim 1, claims 10 and 12 depend from claim 8 and claim 18 depends from claim 15, which Applicants have argued *supra* to not be unpatentable over Morishita et al. under 35 U.S.C. §102(b), Applicants maintain that claims 5, 10, 12 and 18 are likewise not unpatentable over Morishita et al. in view of Mancatis and further in view of Shyr et al. under 35 U.S.C. §103(a).

Further as to claims 5 and 10, the Examiner has stated " the **modified** Morishita et al.'s reference shows all the limitations of the claim except for fuse circuit controls the DAC. However Shyr et al.'s figure 1 shows fuse circuit 14 controls the DAC."

Applicants respectfully maintain that the Examiner's argument with respect to Shyr et al. is an improper modification of the secondary reference of Maniatis. The Examiner argues that, the primary reference of Morishita et al. discloses a current mirror. The Examiner also argues that the secondary reference of Maniatis has modified the primary reference of Morishita et al, by alleging that Maniatis teaches or suggests current mirror (a DAC) including an adjustable current source. The Examiner additionally argues that the secondary reference of Shyr et al. has modified the secondary reference of Maniatis, by alleging that Shyr et al. teaches or suggests providing fuses to control the DAC of Maniatis. Applicants maintain that it is improper to argue that a claim feature is taught or suggested by a secondary reference through modification of

another secondary reference. If the Examiner could modify a secondary reference in the preceding manner, then the Examiner would be able to show the existence of any element or feature of any claim merely by chaining a sufficient number of secondary references together in the preceding manner. Accordingly, Applicants respectfully maintain that the rejection of claims 5 and 10 under 35 U.S.C. §103(a) are improper and should be withdrawn. Since the Examiner has not stated a reason for the rejection of claim 18, Applicants contend the argument *supra* with respect to claims 5 and is applicable to claim 18 and the rejection of claim 18 should be withdrawn.

Further, as to claim 12, the Examiner states that "it is seen as an obvious design preference to select the current of known value is to be about equal to the tunneling leakage current of a worst-case process integrated circuit chip dependent upon particular environment of use to ensure optimum performance.." Apllicants contend the Examiners rejection is improper because there is no suggestion in the prior art to combine the references as required by *Karsten Mfg. Corp. v. Cleveland Gulf Co.*, 242 F.3d 1376, 1385, 58 U.S.P,Q.2d 1286, 1293 (Fed. Cir. 2001) which states " In holding an invention obvious in view of a combination of references, there must be some suggestion, motivation, or teaching in the prior art that would have led a person of ordinary skill in the art to select the references and combine them in the way that would produce the claimed invention." The alleged motivation does originate from prior art but has been supplied by the Examiner. Therefore, the Examiner has not established his prima facie case of obviousness. Based on the preceding arguments, Applicants respectfully maintain that claim 12 is not unpatentable over Morishita et al. in view of Mancatis and further in view of Shyr et al and is in condition for allowance.

As to claim 11, the Examiner states that "Morishita et al. "Morishita et al.'s figures 6 and 7 show all the limitations of the claim except the step of performing a burn-in of the integrated circiot chip while forcing the current of known value through a tunneling current leakage monitor device. However it is notoriously well known in the art that burn-in test is for censuring the circuit operates properly in a high voltage condition." Applicants contend Morishita et al. does not teach all the limitations alleged by the Examiner based on Applicants argument supra with respect to the 35 U.S.C. §102 (b) rejection of claim 8 from which claim 11 depends. Further, applicants respectfully inform the Examiner that any person of ordinary skill in the art knows the purpose of burn-in is to accelerate fails not to ensure the circuit operates at high voltage.

As to claim 14, the Examiner states "it is inherent that the first value of the current in a burn-in operation of the integrated circuit is higher than a second current value in a normal operation because the supply voltage in a burn-in operation is higher than the supply voltage in a normal operation." Applicants respectfully inform the Examiner that any person of ordinary skill in the arc knows current in burn-in is not higher than the current during normal operation and further the Examiner seems to have confused the current through the leakage device (the current of known value) with the current drawn by the circuit during burn-in.

As to claims 6 and 19, since claim 6 depends from claim 1 and claim 19 depends from claim 15, which Applicants have argued *supra* to not be unpatentable over Morishita et al. under 35 U.S.C. §102(b), Applicants maintain that claims 6 and 19 are likewise not unpatentable over Morishita et al. in view of Stubbs under 35 U.S.C. §103(a).

As to claims 7, 9 and 20, since claim 7 depends from claim 1, claim 9 depends from claim 8 and claim 20 depends from claim 15, which Applicants have argued *supra* to not be

unpatentable over Morishita et al. under 35 U.S.C. §102(b), Applicants maintain that claims 7, 9 20 are likewise not unpatentable over Morishita et al. in view of Ngo et al. under 35 U.S.C. §103(a).

Further, the Examiners states "Morishita et al/s' figures 6 and 7 show all limitations of the claim except for the leakage monitor device is a gate capacitor. However, Ngo et al.'s figure 2 shows a voltage generating circuit having a capacitor (C1) coupled to the input of the buffer circuit (OA1) in order to filtering noise at the input of the buffer circuit. It is well known in the art that gate capcitor is more compact than regular capacitor. Therefore, it would have been obvious to one having ordinary skill in the art to add a gate capacitor coupled to the input of Morishita et al.'s buffer circuit for the purpose of filtering noise. Thus, the newly added capacitor is part of the leakage monitor device.

Applicants contend that claims 7, 9 and 20 are not obvious in view of Morishita et al. in view of Ngo et al because Morishita et al. in view of Ngo et al. does not teach or suggest every feature of claims 7, 9 and 20. As a first example, Morishita et al. in view of Ngo et al. does not teach or suggest "wherein said leakage monitor device is a gate capacitor." Applicants respectfully point out the following Examiner errors:

1. There is no teaching in Ngo et al. that capacitor C1 is a gate capacitor.

2. Nago et al. teaches in col. 6 lines 40-41 that "capacitor C1 is a 10 picroferrad (read as picofarad) capacitor" which is of too large a value to be obtained from a gate capacitor.

3. The capacitor C1 of Nago et al. is a filtering capacitor whose purpose is to provide a charge reservoir for a reference node, which by its very nature is designed not to tunnel current across its dielectric since if it did tunnel or leak it would alter the voltage appearing on the that

node. Therefore the capacitor C1 of Nago et al. were used to replace the gate capacitor of Applicants invention, it would render Applicants invention non-functional.

4. As in Mashita et al., there is no mention of tunneling leakage current, no less gate tunneling leakage current in Nago et al.

5. Applicants content that there is no noise to filter between the current mirror and voltage buffer of Applicants invention, thus there is no incentive to combine the references for the purpose of "filtering noise" as the Examiner alleges.

Based on the preceding arguments, Applicants respectfully maintain that claims 7, 9 and 20 is not unpatentable over Morishita et al. in view of Ngo et al and are in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0457.

Respectfully submitted,
FOR: Abadeer et al.

Dated: 03/21/2005

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